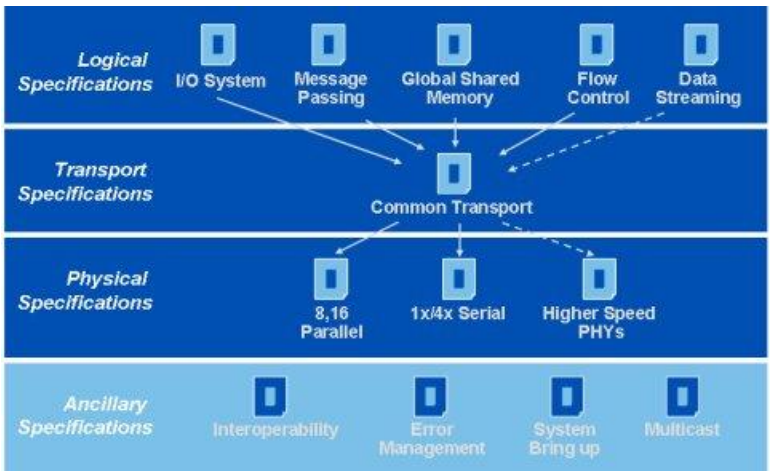
ACCRETE
Growing Together Globally

Serial Rapid Input Output

Contents

RapidIO researchers started to set standards by using Motorola and Mercury Computer System in 1997. Its goal is to try to break the standard which is set in 1999. In 2001, the regulations were completed. The System logical objects, FPGA and ASIC chips have achieved this technology and several companies have achieved mass production. In October 2003, the International Standards Organization and the International Electrical and Electronic Commission (IEC) unanimously adopted the RapidIO Interconnect Specification. (I.e. ISO / IEC DIS 18372) Since then, RapidIO (ISO) has become the only authorized systems of interconnecting technology. Although the RapidIO standard has been adopted for about 8 years, but it still provide engineers with high-speed, advanced communication technology: it still supports many integrated circuits, boards, backplanes and computer system.

The following are the manufacturers that acquired the standards of RapidIO :



Freescale Semiconductor, Lucent-Alcatel, PMC-Sierra, Texas Instruments, Tundra Semiconductor and WindRiver, etc. Now, engineers have more than a hundred products that is based on RapidIO to choose from, these products cover a vast variety of development tools including embedded systems, intellectual property, software, test and measurement equipment and semiconductor (ASIC, DSP, FPGA), etc.

RapidIO standard defines three structural layers: the logical layer, transport layer and physical layer. Logical layer defines the protocol, packet formats, initiating signals and ending signals. Transport layer provides path that allows information can transmit to each nodes. The physical layer describes the packet transmission, information control, electrical characteristics and operational error. The Layered-structure not only keeps the producpt competitive in the market but also increase the capacity of the product.

In the physical layer, RapidIO is a full-duplex serial connection by using the 10-Gigabit Ethernet Attachment Unit Interface (XAUI) also called zowie which fits to IEEE 802.3. "XAUI": the "X" means 10Gbps, the electrical interface work on the 1.25GHz, 2.5GHz or 3.125GHz frequency, after recoded by 8b/10b, it can reach 2.5Gbps.

XAUI has two versions: one-lane and four-lane. Four-lane provides a full-duplex communication with10Gbps interface. Serial RapidIO (SRIO) interface provides the interface from 10Gbps to1Gbps which gives designers a lot more flexibility when it comes to design.

In order to connect two kinds of serial and parallel interconnect, RapidIO standard set standard programming models. They are Addressing Mechanisms and Transactions. These models include basic memory mapped I / O and universal consistency memory. RapidIO is

able to detect the advanced error and provide error reporting and recovery the transmission channels. Each packet includes Cyclic Redundancy Check (CRC).

Through the PCI and PCI-e (serial PCI), RapidIO specification is able to perform one by one load/store operations. RapidIO has developed a package agreement to handle Ethernet packets. When the designers are using the RapidIO switch signal transfer bus structure in an Ethernet network, it will improve system's performance. RapidIO software working group is developing a standards models, this model will enhance the next generation of PCI Express system. The latest RapidIO specification (1.3) adds advanced multicast data flow enhancements, mainly in response to these additional specifications. They are 5Gbps and 6.25Gbps.

In addition, RapidIO Interconnect Specification is compatible both parallel and series systems. Rapid IO can convert serial to parallel without any agreement. What's more, Rapid IO exchange can sustain several serial and parallel, because they are different only in the physical layer. As Rapid IO Trade Association issues the regulations about information flow control and process specifications, RapidIO embedded interconnect is already stand by for its task.

High-performance embedded, communications, active RapidIO

RapidIO interconnects structure mainly aimed to solve the reliability and high performance embedded system's connective challenges. As a system-level interconnect, RapidIO interconnect can be applied on many occasions: DSP connection, processors and other devices point the subordination connection, control and data backplane connections that connects the baseband and RF boards, chips and processing connection. These applications confirm the RapidIO interconnection's capabilities which also include: wireless infrastructure devices, network access equipment, multi-service platform, high-end routers, storage devices, signal and image processing, military and aerospace applications, industrial computing, scientific computing.

Applications of RapidIO in embedded system

RapidIO Interconnect provides a high bandwidth, low latency for embedded system design. In addition, it has less pin so that it can make full use of the board space. RapidIO technology has transparent to the software that allows any data protocol. It also debugs by providing mechanisms and peer self-built structure to exclude a single point of failure. This will meet the reliability needs of embedded design. As a certified ISO standard, RapidIO interconnect provides a wide range of applications for the system. Interconnect is the key to next-generation's system.

Embedded devices typically adopt distributed processing model of SOC components, integrated process systems and interface features. It requires a large number of systems together to complete the task. There is usually one CPU on one computer. Systems like, PCI-X and PCI Express interconnect are sufficiently support desktop because their hierarchical address space mode. However, the computer interconnect technology re-ported embedded applications can not meet the unique needs of the SOC. In terms of distributed processing systems, RapidIO's point to point interconnect structure provides a good model systematical structure. Its features are: low overhead, hardware support for memory mapping and information support for dialogue between the device and other functions. In addition, RapidIO

is an effective way to peer communication on the Internet. Its performance rate can up to 1-60Gbps, while only possessing a small amount of CPU. RapidIO can be used with many different traffic-management device interface, or bridge to other computing environments. The **syntax** of the logical layer consists data flow, network processor forum, General exchange (CSIX) specifications and network flow processor interface (NPSI) specification. This allows the terminal may have the smallest chip pin to apply to particular traffic management objects.

RapidIO structure is easy to store and bridging protocols, network processing structure, general-purpose processors. This diversity of applications can lower the interoperable costs of data transmission. For example, Ethernet and ATM interworking can be effectively managed in a group of shared memory between processors and data packets by RapidIO structure. RapidIO features on the interoperability indeed encouraged terminals using RapidIO interface. Therefore, simplify the board-side design will become more and more common in communication device, like RapidIO.

PCI Express

Intel formally introduced the PCI Express on IDF in spring 2001. PCI bus is replacing the first-generation I \ O technology, it's also known as 3GIO. Intel support AWG (Arapahoe Working Group) is responsible for the bus specification. On April 17, 2002, AWG finished 3GIO 1.0 draft and hand in the draft to PCI-SIG for a review. At the beginning we all considered it would be named as Serial PCI (Serial ATA by the impact), but in the end he it was officially named the PCI Express. In 2006, Spec2.0 was officially launched (2.0 specification). PCI Express is now widely used in computers, mass storage, etc.

PCIe is a two-way connection that based on the point to point sequence connection (1-bit), which is called "transmission channel." Compare to PCI connector, PCI bus is based on one-way 32-bit parallel bus. PCIe has multi-protocol layer which consists of a dialogue, a data exchange layer and a physical layer. Physical layer can be further divided into logical sub-layer and the electrical sub-layer. Logical sub-layer can be divided into physical code sub-layer (PCS) and medium access control sub-layer (MAC).

Physical Layer

In terms of electricity, each two-way line using low voltage differential signaling (LVDS) which can accumulate to 2.5 trillion Potter totaled. Sending and receiving different information will be transmitted by different channels. Each channel is able to operate four signals. The connection between two PCIe is called "link", which will form up one group of transmission channels or more. All equipment at least supports one transmission channel (x1) link. 2,4,8,16,32 channels are also qualified to have links. This actually provides a better compatibility for a two-way communication. PCI-Express cards including transmission, controlling interruption, and also facilitating compatibility with PCI. There is also a feather called “data stripes” which implies more transmission channel than usual transmitting information between interleaved. But it also comes with another concern that the more information transmitting activities are going on the stronger the hardware support for synchronization of continuous data is required. Just like the other high-speed digital transmission protocol, clock information must be embedded in the signal. In the physical layer, PCIE2.0 standard using common 8B/10B code to approach and ensure a continuous string of 1's and 0 lengths fits the standard. After that the Coding scheme adopts 10 bits instead of 8-bit encoding to transmit data, it taking up 20% of the total bandwidth.

Date Linking Layer

Data Linking layer using Transaction Layer Packets, also TLPs to protect CRC (which is generated by the exchanging floor under 32 byte loop redundancy code) (in this article we are referring LCRC). By Ack and Nak signaling packet, TLPs will be able to pass through the continuity check by LCRC, it's called "Ack" (command correct answer); if it did not pass validation we will call it "Nak" (no response). All the information that is not validated by TLPs or TLPs will be retransmit and stored in the Linking Layer waiting for the re-validation. This ensures that all the transmission will be kept away from white noise. Ack and Nak packet signal were transmitted by the lower layer in the packets which are called data linking layer information packet (Data Linking Layer Packet, DLLP). It used to send and exchange the information of control flow between layers and future to control the power management functions.

Exchanging Layer

PCI Express uses separate responding and submitting. It can guarantee all the transmission will be responded. It adopts the credibility flow controlling system. In this system, a broadcast device can receive initial credible signal and save them into storage. The other device will keep sending out signals at the same time it will detect the available date quota. Once it the signal reaches its highest level, the information will be successfully transmitted. After receiving the end signal all the transmitted information will be disposed in the storage in TLP, it later on will send back to the original sender a greater credibility than the initial one. The first generation PCIe claims that they support every one-way transmission channel and the transfer rate is up to 250 megabytes per second. This rate is based on of 2500 MPotter divided by the encoding rate (10 byte / person per group). This means that a 16-channel (x16) PCIe card can theoretically achieve 4000 (250x16) million bytes / second (3.7G megabytes / second) just for a one-way communication. In fact, the actual data transfer rate is according to the payload rate, which means it depends on the characteristics of the data itself. It also included the higher level (software) application and intermediate protocol layer decision. PCI Express depends on the transmission robustness (Robustness) (CRC checksum algorithm Ack).When it comes to continuous and time consuming transfer (such as high speed storage devices) will cause PCIe channel being occupied for over 95%(> 95%). However, most of transmission devices such as USB or Ethernet controller will transfer the content after splitting them into smaller data packets, but reducing the efficiency of the transmission channel. In general, this kind of efficiency reduction is not only in PCIe.

PCI Express bus technology advantages:

1. Serial bus, point to point transmission, exclusive transmission channel.

2. PCI Express bus supports two-way transmission mode and data sub-channel transfer mode. PCI Express includes x1, x2, x4, x8, x12, x16 and x32 multi-channel connection, each direction is able to achieve 250MB / s, two-way transmission is able to achieved 500MB / s, this is a huge advantage of PCI bus. See Table-1.

3. PCI Express bus adopts the advanced point to point interconnect, packet-based protocol which improves the bus's performance. It also includes Power management, Quality of service (QoS), hot swap support, data integrity and error-handling mechanism.

4. PCI bus has excellent capacity and reliability. The following are PCI and PCI Express bus' key features, such as the application model, storage structure, software interface compatible with the traditional PCI bus, but the parallel PCI bus has been replaced by serial bus.

5. PCI Express has reduced the complexity of hardware platform design which significantly decreases the manufacturing costs. See the table below, the system bus reduced hardware's PIN numbers. .

PCI Express 3.0

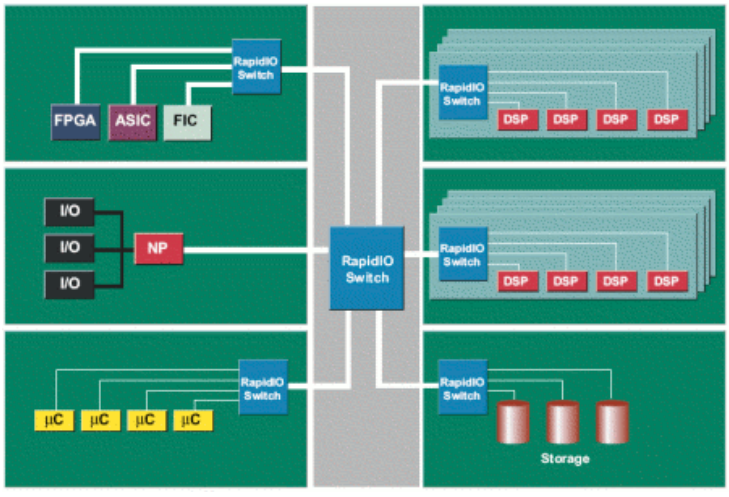
In August 2007, PCI Special Interest Group (PCI SIG) has aimed to reach 8 Giga byte/ s as the next-generation PCI Express's goal. During these months, PCI Group argues about whether Express 3.0 is going to be 8GT / s or 10GT / s. Finally, manufacturing cost has engineers eventually reach a common ground. PCI Express 3.0 also cancel the 8bit/10bit code, removed 20% of the processing overhead, so the real version will be twice than 2.0 which is 5GT / s version

Express 3.0 will use the existing scrambling-polynomial technology to recover clock and solving DC wandering problem. Of course, this method requires the media access controller with additional processing. Studies suggest that the slower rate is more suitable for mainstream chip technology and the current circuit board material. PCI Express 3.0 includes many new features, such as extended signal, data integrity, transmit receive equalization, PLL improvements, clock data recovery and channel expansion. The final specification will be released in late 2009, and the corresponding products will be release in 2010.

In the new version was released, engineers plan based on a number of SIG members develop and test chips for standard analog electrical parameters optimization. It is not clear is the future of on-board interconnection using copper connections or light waves, PCI SIG will conduct more research.

High-speed bus technology: the Future Trend

In the high-end embedded, communications, engineers are going through a war to fight a variety of high-speed bus technology. ASI is a PCI Express communications and embedded systems. As the main promoter of Intel they wish to explore the field of communications routers, switches and storage devices in applications such as design wins bid. However, after years of operation, only a few companies adopt ASI chip, and the future isn't that optimistic. However, the original unintentional Express as a local computing and embedded processor interface flourish, and soon, the PCI Special Interest Group (SIG) began to expand on the Express this is when ASI is be able to get involved. Obviously, Intel is still hoping to come



back to communications field.

In the market, ASI and SIG are different; RapidIO has established strong business alliances with leading OEM manufacturers. Lucent, Ericsson, and storage giant EMC Corp. which has been selected as the representative of RapidIO Trade Federation officials last year. Lucent has also declared their strong bonding with RapidIO, and is less likely cooperating with ASI. And yet, popularity of Express is still possible reversing from this trend. More and more communications are aiming to promote the local Express-chip interface. In fact, even those who invest RapidIO Company has started investing Express. And now these two company start to walk on their own way, each of them has both established great achievements and ensure their authorities separately. For the next generation, communication systems require multiple connections on the backplane processing card, chip manufacturers, all kinds of Ethernet, Infiniband, PCI Express and RapidIO chips. We may only say that competition has just only begun.